Remote Lecture on an FPGA-Implementation of Lane Detection

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Learning Objectives

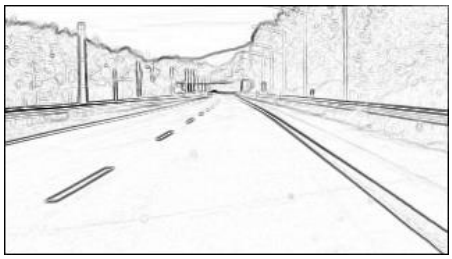
The remote lecture consists of video lectures, an FPGA remote lab and source code in C and VHDL. With the lecture you learn:

- Algorithm development considering a hardware implementation
- Conversion of an algorithm to a digital circuit description
- Simulation of a VHDL description to verify correct design
- Implementation of a complex design on an FPGA

The lecture is intended for advanced students who have first experiences with VHDL design and FPGA implementation. Some knowledge about C programming is helpful.

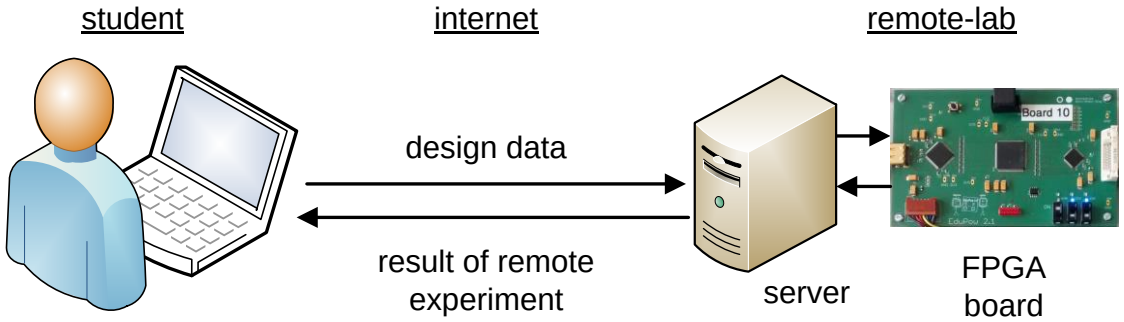
Lane Detection for Vehicles

The lecture deals with lane detection for road scenes which can be part of a lane detection algorithm for vehicles. Lane detection is frequently used in image analysis and has significance for autonomous driving, lane departure warning systems, and traffic sign recognition. The figure shows a road scene and the result of a lane detection algorithm.



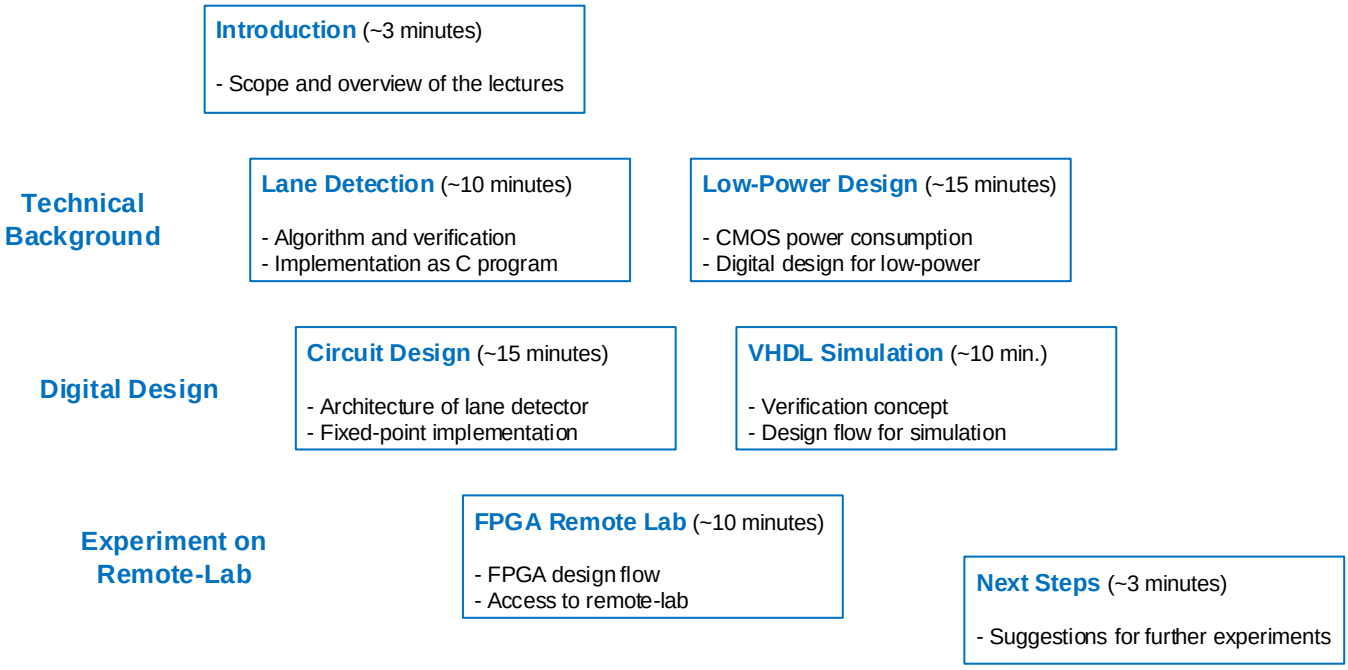
Remote-Lab and Video Lectures

FPGAs are well suited for the implementation of image processing algorithms as they provide high throughput and processing power. You can implement the lane detection algorithm on an FPGA provided in a remote lab. We provide Altera/Intel Cyclone IV and V.



VHDL files are provided and can be modified. The design flow is performed with Altera/Intel Quartus Prime software on your computer and you can send the binary file for the FPGA configuration to the remote lab. As input signal choose a provided road scene or upload your input image for processing. The remote lab is situated in the Bonn-Rhine-Sieg University and the remote server programs the FPGA board, provides the input image and records the result of the experiment. After about 30 to 60 seconds the resulting image plus measurements of power consumption are sent back to you. To ensure high availability of the remote lab a second installation at an independent location is provided.

Video lectures are provided in seven videos, each between 5 to 15 minutes long. You can select the videos to watch and their order based on your interest and previous experience.



Lecture Content

The remote lecture consists of:

- Seven video lectures, each between 3 to 15 minutes duration
- C-code for the lane detection algorithm
- VHDL-code and constraint-files for Altera/Intel-FPGAs
- Sample images for verification
- Access to a remote lab with an FPGA-board
- Information sheet (this document) and list of resources (1 page PDF)

Lecturer

Marco Winzker has developed ASICs and FPGAs as design engineer and group manager for several companies. He is now professor for digital design at the Bonn-Rhein-Sieg University in Germany. He received the IEEE William E. Sayle Award for Achievement in Education 2015 and is fellow of the Stifterverband for innovation in e-teaching. He is coauthor of a German language textbook on digital design.

Availability

The lecture is available at our website: http://h-brs.de/fpga-vision-lab

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